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EXAMINER	
PATEL, ASHOKKUMAR B	

ART UNIT	PAPER NUMBER
2154	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/746,487	TU ET AL.	
	Examiner	Art Unit	
	Ashok B. Patel	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 are subject to examination.

Response to Arguments

2. Applicant's arguments filed July 19, 2004 have been fully considered but they are not persuasive for the following reasons:

a. Examiner would like to present the teachings of the reference Derrick in details exactly as taught by the reference before addressing the Applicant's arguments regarding the teachings of the reference.

Below are the two figures and their corresponding description along with figure elements' capabilities taught by the reference are of a paramount importance since they are in absolute relevancy to the claimed elements.

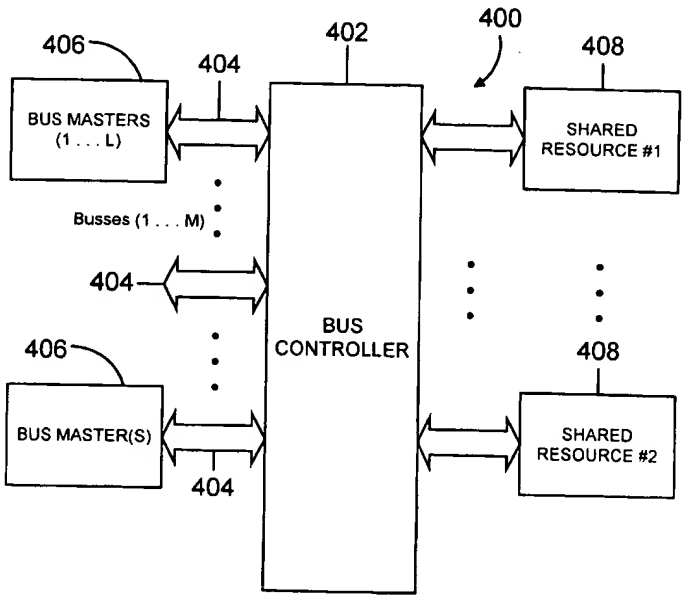

FIG. 4

The reference Derrick teaches "Referring to FIG. 4, a circuit 400 in accordance with the present invention allows concurrent accesses to different semaphores by different devices, and comprises a bus controller 402, one or more busses 404, one or more bus masters 406 on each bus 404, and one or more shared resources 408. Bus controller 402 controls accesses by bus masters 406 to shared resources 408, allowing only one bus master 406 to have control or ownership of any given shared resource 408 at any given time. Bus masters 406 are suitable devices that need access to one or more shared resource 408, and which are capable of obtaining exclusive ownership of one or more shared resource 408. Shared resources 408 are resources, such as random access memory (RAM), that are shared between bus masters 406. Bus controller 402 may control accesses by bus masters 406 to shared resources 408 using any suitable scheme. For example, bus controller 402 may include arbitration logic which determines when to grant access to a shared resource 408 to a bus master 406. Bus controller 402 may thus assign bus masters 406 a priority which determines the order of granting their requests for shared resources 408. Bus masters 406 may request access to a shared resource 408, or in the alternative may be polled by bus controller 402 to determine whether access to a shared resource 408 is required. Whatever the implemented protocol, bus controller 402 assures data integrity in shared resources 408 and provides for concurrent accesses to different semaphores by different bus masters 406. (col.4, lines 30-56).

Please note the flexibility afforded by the reference in choosing arbiter's arbitration logic.

Below shown is the interior detail of Fig.4's element "Bus Controller" (and only that of Bus Controller) which includes an arbiter implemented as described above for Fig.4.

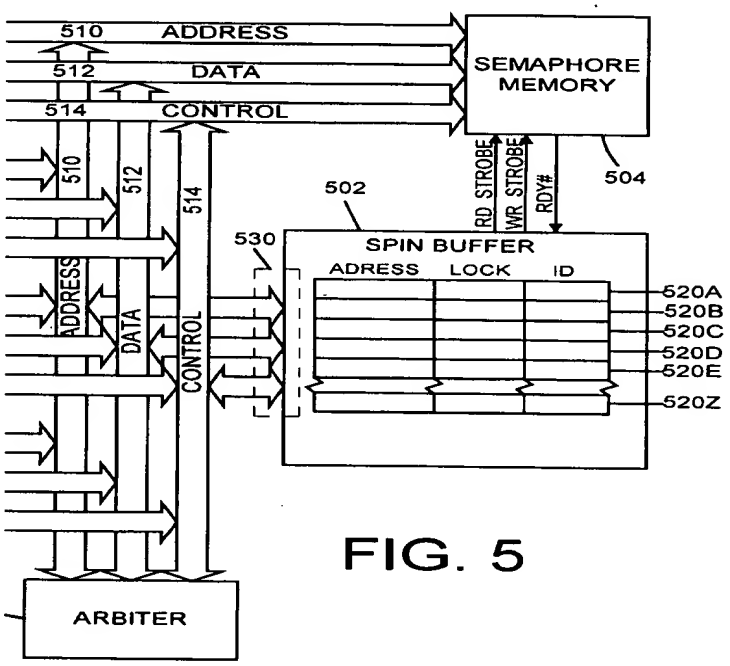

FIG. 5

The reference teaches "Note that spin buffer 520 has the flexibility to discriminate between individual bus masters (e.g., 406A-406D), or in the alternative, may simply discriminate based on the port on which the device is connected. For example, in the circuit of FIG. 6, spin buffer 502 has a separate ID for each device 406A-406D on port 530, but has a single ID for port 540. Thus, if either of devices 406E or 406F have

ownership of a shared resource, the ID that is reflected in the ID field reflects that a device on port 540 has ownership, without distinguishing between the different devices coupled to port 540. Thus, bus master 406A-406D each have a dedicated ID, while bus masters 406E and 406F share an ID. The embodiment as shown in FIG. 6 illustrates that spin buffer 530 may discriminate between individual devices or between ports or between any combination of the two. " (col.5, line 61 through col.6, line 9).

Please note that the spin buffers "discrimination" capabilities are derived from the "arbiter"

Referring to claim 1,

b. In response to Applicant's argument that "Applicant respectfully disagrees with the Examiners assertions. Even if a priority ordering such as round robin was used to order modification request, the combination does not arrive at the present claimed invention.", Applicant is reminded to note the rejection provided wherein claim 6 is pronouncing ", The article of manufacture recited in Claim 1 wherein arbitration is resolved on a round-robin basis." is grouped along with claim 1 with an understanding that priority ordering in accordance with round robin is possible. Denying the use of a mechanism such as round robin, which is already claimed, for ordering modification request is claiming "impossible" article of manufacture. Is it true?

c. In response to Applicant's argument that "The cited references do not disclose or suggest causing a machine that receives the semaphore modification requests to identify an ownership state of the semaphore and to allow the first modification request to succeed if the identified ownership state corresponds to the first

requesting device.", the reference Derrick teaches the arbiter, and by the flexibility afforded by the reference's teaching, as previously indicated, the modification requests are made to succeed as desired.

d. In response to Applicant's argument that "Derrick's device simply locks out accesses by other requesting devices to the same semaphore without knowing if it is owned by another master. It is the requesting device of Derrick, rather than a machine to receive the requests, that checks to see if the shared resource is owned by another device (Fig. 2, steps 204 and 206, col. 3, lines 57-64).", Applicant is interposing the "prior art" deficiencies described in the reference with the solution provided to the deficiencies taught by the reference. In fact the reference teaches "Therefore, there existed a need to selectively disable accesses to a semaphore that is currently being accessed by one bus master while allowing accesses to all other semaphores. This method of resource allocation enhances throughput by allowing different masters to access different semaphores simultaneously. (col.2, lines 53-58).

Also, in response to the Applicant's argument "In contrast, access to a semaphore of Derrick needs to be locked and unlocked by the requesting device to guarantee exclusive access and to allow another device to perform a semaphore operation--even to allow a device that currently owns the desired shared resource to relinquish ownership (col. 2, lines 33-37; Fig. 2, step 208, col. 3, line 67 through col. 4, line 2). On the other hand, a machine that receives the semaphore modification requests, as set forth in Claim 1, identifies an ownership state of the semaphore, can arbitrate the requests and identify a modification request from a first processor to allow

to succeed if the ownership state corresponds to the first processor.", whether a lock or locks of Derrick is/are required must not be viewed as any differentiating element as part of the reference's teaching in establishing the relevancy, direct or indirect, since there is no concrete mention made; indicated, stated, or described, about the "lock or locks" in the claim.

Referring to claim 17,

For responses to all arguments regarding this claim, please refer to the comments provided regarding the teachings of the reference Derrick for claim 1 above.

Referring to claim 8,

For responses to all arguments regarding this claim, please refer to the comments provided regarding the teachings of the reference Derrick for claim 1 above.

Referring to claim 14,

In response to Applicant's argument "While\e Applicant intends that the broadest reasonable interpretation should be given to claims 1-13 and 17-30, the means-plus-function form of claim 14 may not be modified by Applicant with language containing sufficient structure, material or acts for achieving the specified function. Therefore claim 14 should be construed to cover the corresponding structure, material or acts described in the specification and equivalents thereof.", Applicant is reminded that it is the claims that define the claimed invention, and it is claims, not specifications that are anticipated or unpatentable. *Constant v. Advanced Micro-Devices Inc.*, 7 USPQ2d 1064.

For responses to all other arguments regarding this claim, please refer to the comments provided regarding the teachings of the reference Derrick for claim 1 above.

Claim 14 is a claim to a multiprocessor system that carries out the method steps of claim 8, which is implemented in an article of manufacture of claim 1. As such, claim 14 should be viewed to face the same reasons for rejections as those of claim 8 as well as claim 1.

Referring to claim 24,

In response to Applicant's argument regarding this claim, first of all, as indicated above, whether a lock or locks of derrick is/are required must not be viewed as any differentiating element as part of the reference's teaching in establishing the relevancy, direct or indirect, since there is no indicated, stated, described or inferred mention made concretely about the "lock or locks" in the claim. Second, as explained above, Semaphore memory holds the semaphore for the entire set of resources (Fig.6, element 504). Spin buffer is a semaphore checker (Fig.6, element 502, spin buffer) that is coupled to arbiter is a resource scheduling device and the semaphore (Fig.6, element 504, semaphore memory). The arbiter is a resource scheduling device that is coupled to the logical plurality of processing devices (Fig.6, element 506). Spin buffer thus provides the information within the semaphore relating to the ownership status of the shared resource. (col.3, lines 3-5).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Derrick et al. (hereinafter Derrick) (US 5,872,980) in view of Dao et al. (hereinafter Dao) (US 6,148,395).

Referring to claims 1, 2, 3, 6 and 7,

1. A article of manufacture including one or more machine-accessible medium having executable code stored thereon which, when executed by a machine, causes the machine to:

receive one or more semaphore modification requests from one or more requesting devices;

identify an ownership state of a semaphore corresponding to the one or more semaphore modification requests;

arbitrate to identify a first modification request of the one or more semaphore modification requests, the first modification request from a first requesting device;

allow the first modification request to succeed if the identified ownership state corresponds to the first requesting device; and

allow the first modification request to succeed if the identified ownership state corresponds to no ownership.

2. The article of manufacture recited in Claim 1 which, when executed by a machine, further causes the machine to:

decline a second modification request of the one or more semaphore modification requests.

3. The article of manufacture recited in Claim 1 which, when executed by a machine, further causes the machine to:

receive a semaphore read requests from one of the one or more requesting devices;

transmit the identified ownership state in response to the semaphore read request; and

allow the first requesting device to access a shared resource.

6. The article of manufacture recited in Claim 1 wherein arbitration is resolved on a round-robin basis.

7. The article of manufacture recited in Claim 1 wherein arbitration is resolved on a priority basis.

Derrick teaches the spin buffer where the lock and identification data within the semaphore is cached in a multiprocessor environment. (Abstract). Spin buffer thus provides the information within the semaphore relating to the ownership status of the shared resource. (col.3, lines 3-5). When the devices (fig.5, Bus Masters, 406A, 406B, 406C, and 406D) need access to a shared resource and after they initiate the read for the ownership (requests for semaphore modification), spin buffer detects (receives) the read for ownership from the devices. Spin buffer then identifies the ownership state of a semaphore corresponding to the requests (col. 5, lines 34-39). If the semaphore is owned by another device , the requesting device is denied access to the shared resource (declining second modification request). If the requested semaphore is not

owned by another requesting device, then the requesting device can read the data from the semaphore which completes the process of acquiring the ownership of the shared resource (transmitting the identified ownership state and allow the first requesting device to access a shared resource) (col.4, lines 3-9) . Bus controller along with Spin buffer also provides arbiter which determines whose and when to allow the request for resource ownership to succeed based on the priority and availability of a shared resource (Fig. 4, element 402 (Bus Controller), Fig.5, element 506 (Arbiter), col.4, lines 43-56). Although, the reference Derrick teaches that the first modification request is allowed to succeed if the identified ownership state corresponds to no ownership, and indicates that Bus controller (Arbiter) assigns a priority which determines which semaphore modification request is allowed, the reference fails to explicitly teach to allow the first modification request to succeed if the identified ownership state corresponds to the first requesting device, however it is well known in the art to implement the desired protocol for the priority determining the order of granting the requests for semaphore modifications such as round robin. Therefore, it would have been obvious for one in ordinary skill in the art at the time the invention was made to design a means which causes machine to receive the requests for semaphore modifications, to identify an ownership state of a semaphores corresponding to semaphore modification requests, arbitrate and allow the modification requests to succeed as desired, in this case the first modification request to succeed if the identified ownership state corresponds to the first requesting device. Because, it is economical and efficient to share a resource among multiple processors rather than each processor is having a complete set of resources.

Referring to claims 4 and 5,

4. The article of manufacture recited in Claim 1 wherein the semaphore is stored in a multiprocessor comprising the one or more requesting devices.

5. The article of manufacture recited in Claim 4 wherein the multiprocessor comprising the one or more requesting devices is integrated on a single die.

Keeping in mind the teachings of Derrick as indicated above, Derrick does not teach storing the semaphore in a multiprocessor and multiprocessor comprising the one or more requesting devices integrated on a single chip. Dao teaches the semaphore stored in a multiprocessor and the multiprocessor comprising the one or more requesting devices integrated on a single chip in the environment offering shared resources like floating point unit and cache. The multiprocessor also includes the logic control including arbitration for the use of certain shared resources and for updating status information regarding the current state of the device.(Abstract, Fig.1, col. 3, lines 34-43, col. 11, lines 20-25). Therefore, it would have been obvious for one in ordinary skill in the art at the time the invention was made to integrate the spin buffer, arbiter, and semaphore memory of Derrick for storing the semaphore in a multiprocessor where multiprocessor comprises of one or more CPUs (requesting devices) on a single die as taught by Dao. Because, as inferred by the teaching of Dao, when requesting devices are integrated on a single chip, the chip size is reduced which translates into high manufacturing yield and low per-chip manufacturing cost.

Referring to claims 8, 9,10, 12 and 13,

8. A method comprising:

receiving one or more semaphore modification requests from one or more requesting devices;

identifying an ownership state of a semaphore corresponding to the one or more semaphore modification requests;

arbitrating to identify a first modification request of the one or more semaphore modification requests, the first modification request from a first requesting device;

allowing the first modification request to succeed if the identified ownership state corresponds to the first requesting device; and

allowing the first modification request to succeed if the identified ownership state corresponds to no ownership

9. The method recited in Claim 8 further comprising declining a second modification request of the one or more semaphore modification requests.

10.The method recited in Claim 8 further comprising:

receiving a semaphore read requests from one of the one or more requesting devices;

transmitting the identified ownership state in response to the semaphore read request; and

allowing the first requesting device to access a shared resource.

12. The method recited in Claim 8 wherein arbitration is resolved on a round robin basis.

13. The method recited in Claim 8 wherein arbitration is resolved on a priority basis.

Claims 8, 9, 10, 12 and 13 are the methods associated with the article of manufacture of claims 1,2,3,6 and 7. Therefore claims 8, 9, 10, 12 and 13 are rejected for the reasons set forth in above paragraph for claims 1, 2, 3, 6 and 7.

Referring to claim 11,

11. The method recited in Claim 8 wherein each of the one or more semaphore modification requests received identify a corresponding requesting device of the one or more requesting devices.

Derrick teaches having a separate identification of each requesting devices connected to each port of spin buffer thus Derrick's spin buffer is capable of discriminating between the individual devices when it comes to prioritizing the semaphore modification requests. (col.5, lines 53-67 and col.6, lines 1-9).

Referring to claims 14 and 15,

14. A multiprocessor system comprising:

means for receiving one or more semaphore modification requests from one or more requesting devices;

means for identifying an ownership state of a semaphore corresponding to the one or more semaphore modification requests;

means for arbitrating .to identify a first modification request of the one or more semaphore modification requests, the first modification request from a first requesting device;

means for granting the first modification request if the identified ownership state corresponds to the first requesting device; and

means for granting the first modification request if the identified ownership state corresponds to no owner.

15. The multiprocessor system recited in Claim 14 further comprising:

means for receiving a semaphore read requests from one of the one or more requesting devices;

means for transmitting the identified ownership state in response to the semaphore read request; and

means for allowing the first requesting device to access a shared resource.

Claims 14 and 15 include a multiprocessor system that implement the methods of claims 8 and 10 associated with the article of manufacture of claims 1 and 3. Therefore claims 14 and 15 are rejected for the reasons set forth in above paragraph for claims 1, 2, 3, 6 and 7.

Referring to claim 16,

16. The multiprocessor system recited in Claim 14 wherein the one or more requesting devices are fabricated on a single die.

Claim 16 is rejected for the reasons set forth in above paragraph for claims 4 and 5.

Referring to claim 17,18, 19, 22 and 23,

17.A multiprocessor comprising:

a logical plurality of processors;

a resource scheduling device coupled to one or more of the logical plurality of processors to provide access to a set of resources;

a shared resource of the set of resources having a semaphore;

a semaphore checker coupled to the resource scheduling device and to the semaphore to:

receive one or more semaphore modification requests from the one or more of the logical plurality of processors,

identify an ownership state of the semaphore,

arbitrate the one or more semaphore modification requests and identify a first modification request from a first requesting processor of the one or more of the logical plurality of processors,

allow the first modification request to succeed if the identified ownership state corresponds to the first requesting processor; and

allow the first modification request to succeed if the identified ownership state corresponds to no ownership.

18. The multiprocessor recited in Claim 17 wherein the semaphore checker is further to:

decline a second modification request of the one or more semaphore modification requests.

19. The multiprocessor recited in Claim 17 wherein the semaphore checker is further to:

receive a semaphore read requests from one of the one or more of the logical plurality of processors;

transmit the identified ownership state in response to the semaphore read6 request; and

allow the first requesting processor to access a shared resource.

22. The multiprocessor recited in Claim 17 wherein arbitration is resolved on a round-robin basis.

23. The multiprocessor recited in Claim 17 wherein arbitration is resolved on a priority basis.

Derrick teaches the spin buffer where the lock and identification data within the semaphore is cached in a multiprocessor environment. (Abstract). An arbiter is resource scheduling device that is coupled to the logical plurality of processors (Fig.6, element 506). Semaphore memory holds the semaphore for the entire set of resources (Fig.6, element 504). Spin buffer is a semaphore checker (Fig.6, element 502, spin buffer) that is coupled to arbiter which is a resource scheduling device and the semaphore (semaphore memory). Spin buffer thus provides the information within the semaphore relating to the ownership status of the shared resource. (col.3, lines 3-5). When the logical plurality of processors (fig.5, Bus Masters, 406A, 406B, 406C, and 406D) need access to a shared resource and after they initiate the read for the ownership (requests for semaphore modification), spin buffer detects (receives) the read for ownership from the devices. Spin buffer then identifies the ownership state of a semaphore corresponding to the requests (col. 5, lines 34-39). If the semaphore is owned by another device , the requesting device is denied access to the shared resource

(declining second modification request). If the requested semaphore is not owned by another requesting device, then the requesting device can read the data from the semaphore, which completes the process of acquiring the ownership of the shared resource (transmitting the identified ownership state and allow the first requesting device to access a shared resource) (col.4, lines 3-9) . Bus controller along with Spin buffer also provides an arbiter which determines whose and when to allow the request for resource ownership to succeed based on the priority and availability of a shared resource (Fig. 4, element 402 (Bus Controller), Fig.5, element 506 (Arbiter), col.4, lines 43-56). Although, the reference Derrick teaches that the first modification request is allowed to succeed if the identified ownership state corresponds to no ownership, and indicates that Bus controller (Arbiter) assigns a priority which determines which semaphore modification request is allowed, the reference fails to explicitly teach to allow the first modification request to succeed if the identified ownership state corresponds to the first requesting device, however it is well known in the art to implement the desired protocol for the priority determining the order of granting the requests for semaphore modifications such as round robin. Therefore, it would have been obvious for one in ordinary skill in the art at the time the invention was made to design a means which causes machine to receive the requests for semaphore modifications, to identify an ownership state of a semaphores corresponding to semaphore modification requests, arbitrate and allow the modification requests to succeed as desired, in this case the first modification request to succeed if the identified ownership state corresponds to the first

requesting device. Because, it is economical and efficient to share a resource among multiple processors rather than each processor is having a complete set of resources.

Referring to claim 20,

20. The multiprocessor recited in Claim 17 wherein each of the one or more semaphore modification requests received identify a corresponding requesting processor of the one or more of the logical plurality of processors.

Derrick teaches having a separate identification of each requesting logical processor of the one or more of the logical plurality of processors connected to each port of spin buffer thus Derrick's spin buffer is capable of discriminating between the individual logical processors when it comes to prioritizing the semaphore modification requests. (col.5, lines 53-67 and col.6, lines 1-9).

Referring to claim 21,

21. The multiprocessor recited in Claim 17 wherein the multiprocessor is fabricated on a single die.

Claim 21 is rejected for the reasons set forth in above paragraph for claims 4 and 5.

Referring to claim 24, 25, 26, 27 and 30,

24. An apparatus comprising:

a register to access a shared resource of a set of resources;

a semaphore corresponding to the shared resource; and

a semaphore checker coupled to the semaphore to allow access to the shared resource through the register.

25. The apparatus of Claim 24 wherein the semaphore checker is further to:

receive one or more semaphore modification requests from one or more of a logical plurality of processing devices,

identify an ownership state of the semaphore,

arbitrate the one or more semaphore modification requests and identify a first modification request from a first requesting device of the one or more of the logical plurality of processing devices,

allow the first modification request to succeed if the identified ownership state corresponds to the first requesting device; and

allow the first modification request to succeed if the identified ownership state corresponds to no ownership.

26. The apparatus of Claim 25 wherein the semaphore checker is further to:

decline a second modification request of the one or more semaphore modification requests.

27. The apparatus of Claim 25 wherein the semaphore checker is further to:

receive a semaphore read requests from one of the one or more of the logical plurality of processors;

transmit the identified ownership state in response to the semaphore read request; and

allow the first requesting processor to access a shared resource.

30. The apparatus of Claim 25 wherein arbitration is resolved on a round-robin basis.

Derrick teaches the spin buffer where the lock and identification data within the semaphore is cached in a multiprocessor environment. (Abstract). Semaphore memory

holds the semaphore for the entire set of resources (Fig.6, element 504). Spin buffer is a semaphore checker (Fig.6, element 502, spin buffer) that is coupled to arbiter is a resource scheduling device and the semaphore (Fig.6, element 504, semaphore memory). The arbiter is a resource scheduling device that is coupled to the logical plurality of processing devices (Fig.6, element 506). Spin buffer thus provides the information within the semaphore relating to the ownership status of the shared resource. (col.3, lines 3-5). When the logical plurality of processing devices (fig.5, Bus Masters, 406A, 406B, 406C, and 406D) need access to a shared resource and after they initiate the read for the ownership (requests for semaphore modification), spin buffer detects (receives) the read for ownership from the devices. Spin buffer then identifies the ownership state of a semaphore corresponding to the requests (col. 5, lines 34-39). If the semaphore is owned by another device , the requesting device is denied access to the shared resource (declining second modification request). If the requested semaphore is not owned by another requesting device, then the requesting device can read the data from the semaphore, which completes the process of acquiring the ownership of the shared resource (transmitting the identified ownership state and allow the first requesting device to access a shared resource) (col.4, lines 3-9) . Bus controller along with Spin buffer also provides an arbiter which determines whose and when to allow the request for resource ownership to succeed based on the priority and availability of a shared resource (Fig. 4, element 402 (Bus Controller), Fig.5, element 506 (Arbiter), col.4, lines 43-56). Although, the reference Derrick teaches that the first modification request is allowed to succeed if the identified ownership state

corresponds to no ownership, and indicates that Bus controller (Arbiter) assigns a priority which determines which semaphore modification request is allowed, the reference fails to explicitly teach to allow the first modification request to succeed if the identified ownership state corresponds to the first requesting device, however it is well known in the art to implement the desired protocol for the priority determining the order of granting the requests for semaphore modifications such as round robin. Therefore, it would have been obvious for one in ordinary skill in the art at the time the invention was made to design a means which causes machine to receive the requests for semaphore modifications, to identify an ownership state of a semaphores corresponding to semaphore modification requests, arbitrate and allow the modification requests to succeed as desired, in this case the first modification request to succeed if the identified ownership state corresponds to the first requesting device. Because, it is economical and efficient to share a resource among multiple processors rather than each processing device is having a complete set of resources.

Referring to claim 28,

28. The apparatus of Claim 25 wherein each of the one or more semaphore modification requests received identify a corresponding requesting device of the one or more of the logical plurality of processing devices.

Claim 28 is rejected for the reasons set forth in above paragraph for claim 20.

Referring to claim 29,

29.The apparatus of Claim 25 wherein the logical plurality of processing devices are integrated on a single die.

Claim 29 is rejected for the reasons set forth in above paragraph for claims 4 and 5.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ashok B. Patel whose telephone number is (571) 272-3972. The examiner can normally be reached on 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John A Follansbee can be reached on (571) 272-3964. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

abp
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